# PEC-I interface to ST



## Overview

The PECI interface operates at a nominal voltage set by Vcc ST. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc ST interface supply.

## Key Takeaways

PECI serves as the communication channel between Intel CPUs and system management controllers, enabling configuration and monitoring of Speed Select Technology features.

### Overview of PECI

The Platform Environment Control Interface (PECI) is a proprietary Intel single-wire serial interface that allows external devices, such as Baseboard Management Controllers (BMCs) or Embedded Controllers (ECs), to communicate with Intel processors for monitoring, configuration, and diagnostics purposes.

### PEC

I uses a self-clocking one-wire bus, where each processor package has a unique address, and the interface supports variable data rates from 2 kbit/s to 2 Mbit/s. It provides access to digital thermal sensors (DTS), processor configuration registers, and error/status monitoring registers.

*© 2026 PROMETHEAS OPTICAL - All rights reserved*

## PEC

I and Speed Select Technology (SST)Intel Speed Select Technology (SST) allows administrators to configure CPU performance profiles, core prioritization, and frequency settings on supported Xeon processors.

## PEC

I acts as the communication backbone for SST by enabling the BMC or management software to send commands to the CPU and read responses. Specifically: SST-PP (Performance Profiles): PECI allows the BMC to select different TDP-based performance profiles. SST-BF (Base Frequency): PECI enables configuration of higher base frequencies for selected cores.

SST-TF (Turbo Frequency): PECI facilitates control over turbo frequency behavior, depending on CPU capabilities.

## The SS

T implementation in OpenBMC uses a backend provider pattern where PECI communicates with the CPU via the OS Mailbox interface, and the PECIManager class handles CPU wake states, command sending, and response parsing.

## Software Interfaces

In Linux and OpenBMC environments, PECI support is provided through kernel drivers and D-Bus APIs: Linux Kernel: PECI support is available as a module (peci) and allows access to CPU thermal and configuration registers. OpenBMC D-Bus Interface: SST features are exposed through D-Bus, enabling administrators to query and configure CPU performance settings programmatically or via management tools.

## Practical Use

## Using PEC

I, system management software can: Monitor CPU temperatures and thermal throttling points.

## Adjust CP

U performance profiles dynamically. Access processor configuration and error registers for diagnostics. Implement power and thermal management strategies in server environments.

In summary, PECI provides a low-level, reliable interface for system controllers to manage Intel CPUs, and it is the primary channel through which Speed Select Technology features are configured and monitored in modern server platforms.

*© 2026 PROMETHEAS OPTICAL - All rights reserved*

## Article Content

Overview — The Linux Kernel documentation

PECI Wire interface uses a single wire for self-clocking and data transfer. It does not require any additional control lines - the physical layer is a self-clocked one-wire bus signal that begins each bit

PECI DC Characteristics

The PECI interface operates at a nominal voltage set by Vcc ST. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc ST interface supply.

Platform Environment Control Interface

Platform Environment Control Interface (PECI) is an Intel proprietary single wire serial interface that provides a communication channel between Intel processors and chipset components to external

Speed Select Technology | openbmc/smbios-mdr | DeepWiki

It covers how the BMC interacts with Intel CPU SST features via PECI (Platform Environment Control Interface), exposes them through D-Bus interfaces, and provides tools for

Platform Environment Control Interface (PECI)

The PECI interface allows external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

Command-line Tool | openbmc/libpeci | DeepWiki

This utility allows system administrators, developers, and hardware engineers to execute PECI commands directly from the command line, facilitating testing, debugging, and monitoring of

Linux Kernel Documentation / peci / peci.rst

PECI provides services that allow the management controller to configure, monitor and debug platform by accessing various registers. It defines a dedicated command protocol, where the

Platform Environmental Control Interface

PECI is used for platform thermal management and real-time control and configuration of processor features and performance. Note: PECI over eSPI is supported.

*© 2026 PROMETHEAS OPTICAL - All rights reserved*

linux/Documentation/peci/peci.rst at master · torvalds/linux

PECI Wire interface uses a single wire for self-clocking and data transfer. It does not require any additional control lines - the physical layer is a self-clocked one-wire bus signal that begins each bit

PCIe internal peripheral

The PCIe internal peripheral is based on the Synopsys DesignWare ®PCIe controller. It''s a PCIe Gen2 controller, hence allowing to communicate by using the PCIe Gen1 or Gen2 protocol.

1.1. Cyclone V Avalon-ST Interface for PCIe Datasheet

Altera® Cyclone® V FPGAs include a configurable, hardened protocol stack for PCI Express® that is compliant with PCI Express Base Specification 2.1 or 3.0. The Hard IP for PCI

Altera Arria 10 Avalon-ST PCIe Interface User Guide

Comprehensive guide for implementing PCI Express (PCIe) solutions with SR-IOV support for Arria 10 FPGAs. Provides detailed information on configuration, simulation, and design integration.

Specifications

Specifications PCI-SIG ® specifications define standards driving the industry-wide compatibility of peripheral component interconnects. Members regularly review them, providing commentary and

9.1.1. Avalon-ST Interface

An Avalon-ST interface connects the Application Layer and the Transaction Layer. This is a point-to-point, streaming interface designed for high throughput applications. The Avalon-ST

How does the PCIe protocol stack work?

The Peripheral Component Interconnect Express (PCIe) is a high-speed serial computer expansion bus standard. It''s the common motherboard interface in systems from personal computers

Overview — The Linux Kernel documentation

Overview ¶ The Platform Environment Control Interface (PECI) is a communication interface between Intel processor and management controllers (e.g. Baseboard Management Controller, BMC). PECI

Overview of ST-LINK derivatives

*© 2026 PROMETHEAS OPTICAL - All rights reserved*

Introduction In this document, ST-LINK is a generic name that refers to the different implementations of a debugger/programmer probe interface for STMicroelectronics microcontrollers. ST-LINK is also the

Hello, and welcome to this presentation of the STM32 I²C interface. It ...

Hello, and welcome to this presentation of the STM32 I²C interface. It covers the main features of this communication interface, which is widely used to connect devices such as microcontrollers, sensors,

## Contact Us

Continue your research online:

Website: https://prometheas.fr
Technical inquiry: https://prometheas.fr/project-desk.html
North American project region: Ashburn, Loudoun County, Virginia, United States

This document is for preliminary research. Verify specifications against current standards, product documentation and project requirements.

© 2026 PROMETHEAS OPTICAL - All rights reserved